a semiconductor substrate;

a drain region of a first conductivity type adjacent said semiconductor substrate and comprising a superficial buffer region being more heavily doped than adjacent portions of said drain region;

said superficial buffer region having a dopant concentration of about $5x10^{16}$ to $5x10^{17}$ atoms cm^{-3} and the adjacent portions of said drain region having a dopant concentration of about $2.5x10^{15}$ to $2.5x10^{16}$ atoms cm^{-3};

a body region surrounded by said superficial buffer region and having a second conductivity type; and

a source region in said body region and having the first conductivity type.

REMARKS

The Examiner is thanked for the thorough examination of the present application. The specification has been amended to correct the noted informalities, as helpfully pointed out by the Examiner. Further, independent Claims 5 and 14 have been amended to more clearly define the subject matter thereof over the prior art. Support for the amendments to Claims 5 and 14 may be found on page 5, lines 3-7 of the originally filed specification, and in FIG. 2b of the drawings, for example. No new matter is being added.

Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attached pages are captioned "**Version with Markings to Show Changes Made**."

In view of the amendments and the supporting arguments presented in detail below, it is submitted that all of the claims are patentable.

I. The Claimed Invention

The present invention is directed to a lateral diffused metal oxide semiconductor (LDMOS) integrated device. As recited in amended independent Claim 5, for example, the LDMOS device includes a semiconductor substrate and a drain region of a first conductivity type adjacent the semiconductor substrate and including a superficial buffer region being more heavily doped than adjacent portions of the drain region. Moreover, the LDMOS device also includes a body region surrounded by the buffer region and having a second conductivity type, and a source region in the body region and having the first conductivity type. The LDMOS device thus provides a RESURF structure that may be used at relatively high voltages yet with a reduction in punch through problems.

Independent Claim 14 is directed to a related LDMOS integrated device. This claim has similarly been amended to recite that the body region is surrounded by the buffer region as in Claim 5.

II. The Claims Are Patentable

The Examiner rejected independent Claims 5 and 14 over Lidow et al. As perhaps best seen in FIG. 2 of Lidow et al., this patent is directed to a high power vertical diffused MOSFET **20** in which two laterally spaced-apart n+ sources **32, 33** are controlled by a single gate. Each of the sources **32, 33** supply current through channel regions **34, 35** in respective p+ diffusion regions **30, 31**. The channel regions **34, 35** lead from source electrodes **23, 24** to a relatively low resistivity, epitaxially-formed drain region (n-) which is deposited on a high conductivity substrate **20a**. Immediately adjacent and beneath the gate and in the path from the sources **32, 33** to the drain is a relatively high conductivity n+ region **40**, which reduces the on-resistance of the device. Further, the

breakdown voltage of the device is increased by making the p+ diffusions **30, 31** relatively deep and with a large radius of curvature beneath each of the sources **32, 33**. These relatively deep regions are referred to as "lower bulk" portions in Lidow et al. (see, e.g., col. 2, lines 17-20).

The Examiner contended that the region **40** and the n+ region **86** in the alternate embodiment illustrated in FIG. 8 of Lidow et al. (which is similar to the region **40**) were superficial buffer regions as recited in independent Claims 5 and 14. These claims have been amended to recite that the body region is surrounded by the superficial buffer region. In stark contrast, the n+ regions **40, 86** do not surround their respective p+ diffusions regions **30, 31** and **89, 90**, as is clearly illustrated in FIGS. 2 and 8 of Lidow et al. Nothing in the specification indicates that these n+ regions would, or even could, ever be extended to surround the entire p+ diffusion regions. In fact, Lidow et al. teaches away from doing so. That is, the relatively deep lower bulk portions of the p+ regions **30, 31** and **89, 90** are specifically formed to have a large radius of curvature in contact with their respective n- drain regions to increase breakdown voltage. See, e.g., col. 4, lines 1-15, and the abstract of Lidow et al. To surround the p+ diffusion regions **30, 31** and **89, 90** with the n+ regions **40, 86** would eliminate this necessary area of contact with the n- drain.

Instead, the n+ regions **40, 86** are intentionally positioned beneath the gate oxide **25** and between the channels **34, 35** to reduce the forward on resistance of the device. See col. 4, lines 57-64 of Lidow et al. That is, these n+ regions are positioned along the channels to provide vertical current collection and decrease channel resistance. Yet, to somehow surround the p+ regions **30, 31** and **89, 90** with the n+ regions **40, 86** would decrease the voltage capability of the device,

and thus destroy its operability.

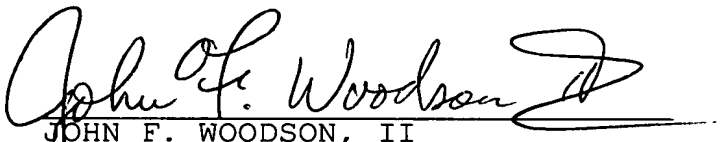
In summary, Lidow et al. fails to teach an LDMOS including a body region surrounded by a superficial buffer region. Moreover, there cannot be any motivation or suggestion to so modify the device of Lidow et al. because to do so would destroy its operability and render the device unsatisfactory for its intended purpose.

Accordingly, it is submitted that independent Claims 5 and 14 are patentable over the prior art. Their respective dependent claims, which recite yet further distinguishing features, are also patentable over the prior art and require no further discussion herein.

CONCLUSIONS

In view of the amendments to the claims and the arguments presented above, it is submitted that all of the claims are patentable. Accordingly, a Notice of Allowance is respectfully requested in due course. Should any minor informalities need to be addressed, the Examiner is encouraged to contact the undersigned attorney at the telephone number listed below.

Respectfully submitted,



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In re Patent Application of:
CROCE ET AL.
Serial No. **09/839,596**
Filing Date: **4/20/01**
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VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the Specification:

The paragraph beginning at page 4, line 30 has been amended as follows:

The present invention provides a relatively simple and effective solution to punch-through (PT) problems that normally limit the performance of known RESURF LDMOS structures when functioning as high side drivers. This is done without introducing substantial changes in the known RESURF LDMOS structure. The invention is directed to a RESURF LDMOS structure that includes a superficial or surface portion (or body buffer region) **15** of the drain well region **12** which surrounds the body region **13**. The body buffer region **15** is preferably more heavily doped than the remaining portion of the drain well region **12**, as shown in FIG. 2b. In the drawings, like numbers are used throughout to refer to similar elements for clarity of illustration.

The table beginning at page 6, line 23 has been amended as follows:

TABLE 1

Region	Dopant	Thickness [μm]	Doping [Atoms cm^{-3}]
p-body (conductivity "P")	boron	0.25-0.75	$5x10^{17}$-$5x10^{18}$
body-buffer (conductivity "N")	phosphorous	0.15-0.45 below junction with p-body	$5x10^{16}$-$5x10^{17}$
drain well region (conductivity "N")	phosphorous	1.5-4.5 below junction with body-buffer	$2.5x10^{15}$-$2.5x10^{16}$

The table beginning at page 7, line 1 has been amended as follows:

TABLE 2

region	Dopant	Thickness [μm]	Doping [Atoms cm^{-3}]
n-body (conductivity "N")	phosphorous	0.25-0.75	$5x10^{17}$-$5x10^{18}$
body-buffer (conductivity "P")	boron	0.15-0.45 below junction with n-body	$5x10^{16}$-$5X10^{17}$
drain well region (conductivity "P")	boron	1.5-4.5 below junction with body-buffer	$2.5x10^{15}$-$2.5x10^{16}$

In the Claims:

Claims 5 and 14 have been amended as follows:

5. (Amended) A lateral diffused metal oxide semiconductor (LDMOS) integrated device comprising:

a semiconductor substrate;

a drain region of a first conductivity type adjacent said semiconductor substrate and comprising a superficial buffer region being more heavily doped than adjacent portions of said drain region;

a body region [in] surrounded by said buffer region and having a second conductivity type; and

a source region in said body region and having the first conductivity type.

15. (Amended) A lateral diffused metal oxide semiconductor (LDMOS) integrated device comprising:

a semiconductor substrate;

a drain region of a first conductivity type adjacent said semiconductor substrate and comprising a superficial buffer region being more heavily doped than adjacent portions of said drain region;

said superficial buffer region having a dopant concentration of about $5x10^{16}$ to $5x10^{17}$ atoms cm^{-3} and the adjacent portions of said drain region having a dopant concentration of about $2.5x10^{15}$ to $2.5x10^{16}$ atoms cm^{-3};

a body region [in] surrounded by said superficial buffer region and having a second conductivity type; and

a source region in said body region and having the first conductivity type.

In re Patent Application of:
CROCE ET AL.
Serial No. **09/839,596**
Filing Date: **4/20/01**

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: DIRECTOR, U.S. PATENT AND TRADEMARK OFFICE, WASHINGTON, D.C. 20231, on this 21st day of November, 2002.